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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,925	YAMAZAKI, HIROSHI	
	Examiner	Art Unit	
	Sarvesh J. Nadkarni	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 08/10/2007.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed September 6, 2007, regarding Application Number: 10/809,925 (hereinafter referred to as "amendment"). No claims have been cancelled, and no new claims have been added Claims 1, 4, 7, 8, 9, 10, 11 and 12 have been amended. Therefore, claims 1-12 are currently pending.

Claim Rejections - 35 USC § 112

1. Claims 4, 6, 8, 11, and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

2. Claim 4, as amended, recites "input parts" which was not described in the specification as originally filed.

3. Claim 11, as amended, recites "same horizontal line" which was not described in the specification as originally filed.

4. Claims 6, 8, and 12 recite "plurality of bits" which was not described in the specification as originally filed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Go (US 6,320,566 B1) hereinafter referred to as Go '566.

7. With regard to claim 11, Go '566 discloses **a timing controller** (see column 4 line 10, "clock signal generator") **for a liquid crystal display device,** (see column 4 lines 1-2) **characterized in that data signals of odd-number dots and data signals of even-number dots** (see column 4, lines 20-24) **are output every horizontal line** (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number dots and even-number dots on the same horizontal line by 180 degrees.** (see FIG. 10 and elements 140 and 150 further described as high and low video data at column 7, lines 1-16 and as illustrated in FIGs 10-12; additionally see column 6, lines 20-25).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566") and further in view of Misawa et al., United States Patent Number: 5,616, 936, Date of Patent: April 1, 1997 (hereinafter referred to as "Misawa '936").

10. With regard to claim 1, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver integrated circuits (ICs) for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver ICs** (see column 4, lines 22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and column 6 lines 22 "first clock signal FD2) **which is equipped in parallel with the first clock signal line** (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse relation with the first clock signal;** (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase

difference) **and a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;**(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100")

11. However, Go '566 fails to teach **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line.**

12. However, Misawa '936 teaches **a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first clock signal line**. (see column 20, lines 15-25, the "source line driving circuit" performs this function).

13. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the source line driving circuit as disclosed in Misawa '936 into the liquid crystal display device of Go '566 because, as disclosed in column 12 lines 17-46 of Misawa '936, equalizing the capacitance reduces the added noise and improves picture quality, both of which are consistently progressive goals within the art

14. With regard to claim 5 as dependent on claim 1, Go '566 discloses **a data signal line for odd-number dots** (see column 4, lines 20-24, "odd data lines") **for transmitting data signals of odd-number dots** (pixel electrodes 26 are attached to the odd data lines) **and a data signal line for even-number dots** (see column 4, lines 20-24, "even data lines") **for transmitting data signals of even-number dots** (pixel electrodes 26 are attached to the odd data lines) **are equipped, and the timing controller outputs the data signals of the odd-number dots and**

the data signals of the even-number dots every horizontal line (see FIG. 6A and 6B described in column 2, lines 46-48 in conjunction with FIG. 10 further described at column 6, lines 20-25) **while displacing the phase between the data signals of the odd-number and even-number dots by 180 degrees,** (see column 6, lines10-14 in conjunction with lines 20-28) **and the data driver ICs input the first and second clock signals** (see column 6, lines 19-25)**, latch the data signals of the odd-number dots with the first clock signal and latch the data signals of the even-number dots with the second clock signal** (see column 6, lines 20-28).

15. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go, United States Patent Number 6,320,566 B1, Date of Patent: November 20, 2001 (hereinafter referred to as "Go '566") and further in view of Jeon et al., (US 6,690,347 B2) hereinafter referred to as "Joen '347".

16. With regard to claim 7 as amended, Go '566 discloses **a liquid crystal display device** (see column 1, lines 10-11) **comprising: a liquid crystal display panel;** (see column 1, lines 34-47) **a plurality of data driver ICs for driving data lines of the liquid crystal display panel;** (see column 3, lines 33-38) **a first clock signal line** (see column 4, line 11, "first clock signal" furthermore see FIG. 10 element labeled "FD1" and column 6 lines 21 "first clock signal FD1) **for transmitting a first clock signal to the plurality of data driver ICs** (see column 4, lines 22-25) **a second clock signal line** (see column 4, line 11, "second clock signal" furthermore see FIG. 10 element labeled "FD2" and column 6 lines 22 "first clock signal FD2) **which is equipped in parallel with the first clock signal line** (see FIGs. 10 and 12, clock signal lines FD1 and FD2 are drawn in parallel) **and transmits a second clock signal which is in reverse**

relation with the first clock signal; (see column 4, lines 10-13, describing the signals having a180 degree phase difference, furthermore, see FIG 11, showing the phase difference) **and a timing controller for outputting the first and second clock signals to the first and second clock signal lines respectively;**(see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **wherein each of the data driver ICs input the first and second clock signals, and can selectively latch data signals with the first or second clock signal.** (see column 4, lines 20-28 describing latching data signals and gates to selectively latch to even or odd lines).

1. However, Go '566 does not explicitly teach **a selection signal, select the first or second clock signal based on the selection signal**. In the same field of endeavor, Joen '347 clearly teaches **a selection signal, select the first or second clock signal based on the selection signal** (see Joen '347 at but not limited to, column 7, lines 35-49 describing a selection start signal as applied and also column 10, lines 23-56).

2. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the selection signal as taught by Joen '347 into the display device of Go '566 because both are within the same field of endeavor, and furthermore, because the design as taught by Joen '347 minimizes the number of external connection terminals through its use of two clock signals in block operation (see Joen '347 at column 2, lines 48-end) a common goal within this art.

3. Claims 9 and 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 and further in view of Jeong (US 6,335,721 B1) hereinafter referred to as Jeong '721.

4. With regard to claim 9, Go '566 discloses **a data driver IC** (see column 1, line 52 "data driver IC 11") **for a liquid crystal display device,** (see column 1, lines 10-11). **a first data latch** (see FIG. 12 element 200, further described at column 6, lines 37-47) **that inputs a first clock signal** (see FIG. 12, FD1) **and latches data signals of odd-number dots with the first clock signal** (see column 6, lines 37-65)**; and data latch** (see FIG. 12, element 200) **that inputs a second clock signal in reverse relation with the first clock signal** (see FIG. 12, FD2, and as described at column 6, lines 37-65, further illustrated at FIG. 11) **and latches data signals of even-number dots with the second clock signal**(see FIG. 12, and further described in column 6, lines 37-65)**.** Go '566 does not explicitly teach **a second data latch.**

5. In the same field of endeavor, Jeong '721 clearly teaches **a second data latch** (see FIG. 4 illustrating first and second latch and FIG. 5, further described at column 3, lines 1-40 and column 4, lines 15-40)**.**

6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the second data latch as taught by Jeong '721 into the device of Go '566 because both are within the same field of endeavor, and furthermore, because the design of Jeong '721 improves image quality by buffering negative and positive polarity video signals (see Jeong '721, column 2, lines 53-57).

7. With regard to claim 10, Go '566 clearly teaches **a data driver IC** (see Go '566 column 1, line 52 "data driver IC 11") **for a liquid crystal display device** (see Go '566 column 1, lines 10-11)**, characterized in that the data driver IC inputs a first clock signal** (see Go '566 FIG. 12, FD1, and as described at column 6, lines 37-65, further illustrated at FIG. 11)**and a second clock signal in reverse relation with the first clock signal** (see Go '566 FIG. 12, FD2, and as

described at column 6, lines 37-65, further illustrated at FIG. 11). **a selection signal** (see Jeong '721 column 4 lines 43-end and continued at column 5, lines 1-8), **select the first or second clock signal based on the selection signal, and a can selectively latch data signals with the first or second clock signal** (see Jeong '721 column 4 lines 61-end and continued at column 5, lines 1-8).

8. Claim12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

9. With regard to claim 12, Go '566 discloses **a timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11) However, Go '566 fails to discloses **a data signal of a dot is consisted of a plurality of bits, and output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

10. Ogata discloses **a data signal of a dot is consisted of a plurality of bits** (see abstract discussing bits), **and output pins** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1) **for data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same**

bit (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1).

11. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 into the data signal line arrangement of Ogata because as disclosed in Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 and Misawa '936 as applied to claim 1 above, and further in view of Toyoshima et al., United States Patent, Patent Number US 6,795,049 B2, Date of Patent: September 21, 2004 (hereinafter referred to as "Toyoshima '049").

18. With regard to claim 2, Go '566 in view of Misawa '936 teaches **the liquid crystal display device according to claim 1.** However, Go '566 in view of Misawa '936 fail to teach the **load means is constructed by equipping dummy terminals to the data driver ICs, and connecting the second clock signal line to the dummy terminals.**

19. However, Toyoshima '049 discloses **the load means is constructed by equipping dummy terminals** (column 5, lines 31-33, describing dummy element) **to the data driver ICs** (see FIG 4, further described in column 7, lines 43-59)**, and connecting the second clock signal line to the dummy terminals** (see FIG 4. further described in column 7, lines 43-59; the second clock line is connected to the dummy lines).

20. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the dummy terminal configuration

of Toyoshima '049 into the display device of Go '566 in view of Misawa '936 because Toyoshima '049 provides for stable operation of the display device and a reduced area of elements outside of the display region (see column 1, lines 55-60).

21. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 in view of Misawa '936 as applied to claim1 above, and further in view of Drake et al., United States Patent, Patent Number 6,339,413 B1, Date of Patent: January 15, 2002 (hereinafter referred to as Drake '413).

22. With regard to claim 3 Go '566 in view of Misawa '936 discloses **the liquid crystal display device according to claim 1,** However, Go '566 in view of Misawa '936 fails to teach **the load means is constructed by containing a capacitor in a terminating circuit.**

23. In the same field of endeavor, Drake '413 clearly teaches **the load means is constructed by containing a capacitor in a terminating circuit** (see Figure 6 element 108 used to reduce or eliminate noise and is connected to ground, furthermore, see column 10, lines 37-40).

24. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate display device of Go '566 in view of Misawa '936 into the drive circuit of Drake '413 because the design of Drake '413 reduces noise in the circuit (see column 10, lines 37-40).

25. With regard to claim 4 and as dependent on claim 3, Misawa '936 discloses having another capacitance value having the **same capacitance value as the input capacitance of the first clock signal input parts of the data driver ICs.** Namely, Misawa '936 clearly discloses equalizing the capacitance of the two clock signal lines with the signal bus, and therefore equating the two clock lines. Therefore it would have been obvious to one having ordinary skill

in the art at the time of invention to have combined the terminal capacitor of Drake '413 into the equalizing capacitance design of Misawa because such a design would further reduce the noise in the circuit (see column 10, lines 37-40 of Drake '413).

26. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Go '566" in view of Misawa '936 and further in view of Ogata et al., Japanese Patent Number JP 407329337A. Hereinafter referred to as "Ogata".

27. With regard to claim 6, Go '566 discloses **the liquid crystal display device according to claim 5, wherein a data signal of a dot is consisted of a plurality of bits and a timing controller** (see column 4, lines 10-13 describing a "clock signal generator"; furthermore described in detail at column 6, lines 20-21 described as a "controller IC 100") **for a liquid crystal display device** (see column 1, lines 10-11). However, neither Go '566, nor Misawa '936 teach **output pins for data signals are arranged so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

28. Ogata discloses **data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1).

29. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 and

Misawa '936 into the data signal line arrangement of Ogata because as disclosed in the purpose portion of the abstract of Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

30. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Go '566 in view of Joen '347 as applied to claim 7 above, and further in view of Ogata.

31. Regarding claim 8 as amended, Go '566 in view of Joen '347 clearly teaches **the liquid crystal display device according to claim 7** (see above). Go '566 in view of Joen '347 does not teach **a data signal of a dot is considered of a plurality of bits, and the data driver IC has input pins for data signals arranged so that the data signal of an odd-number of dot of each color and the data signal of an even-number dot of the same bit are adjacent to each other.**

32. Ogata discloses **a data signal of a dot is consisted of a plurality of bits** (see abstract discussing bits), **and output pins** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1) **for data signal of an odd-number dot of each bit of each color** (see abstract "data signal having odd bits") **of each bit** (see abstract "of one line") **and the data signal of an even-number dot** (see abstract "data signal having even bits") **of the same bit** (see abstract "of one line") **are adjacent to one another** (see demonstrative FIG 1 illustrating odd lines 1, 3...n-1 adjacent to even lines 2, 4... n-1).

33. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the display device of Go '566 in view of Joen '347 into the data signal line arrangement of Ogata because as disclosed in Ogata, the arrangement "reduces the capacity of power source" and "prevents the decrease of image quality level."

Response to Arguments

34. Applicant's arguments filed October 3, 2007 have been fully considered but they are not persuasive. All arguments made regarding claims as substantively amended have been fully addressed above and will not be revisited here. Applicant is therefore redirected to the claims as rejected above.

35. Regarding arguments made in reference to claims 1 and 5, all have been considered but none are persuasive.

36. The first argument on page 10 of Applicant's amendment and continued on page 11, stating "Misawa '936 teaches away from the combination of Go '566 and Misawa '936", is not persuasive.

Misawa '936 is presented for "a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first signal line." Misawa is not introduced to teach "a second clock signal line which is equipped in parallel with the first signal line" as this is clearly taught by Go '566 as described above.

Additionally, Misawa '936 teaches "a load means for making the load capacitance of the second clock signal line equal to or substantially equal to the load capacitance of the first signal line" by "an average distance between CL line 218 and the video signal bus and between CL line 219 and the video signal bus are about equal. As a result, the value of stray capacitance (C_{s1} + C_{s3}), which is formed between the CL line and the video bus is equal to the value of stray capacitance (C_{s2}+C_{s4}) formed between the CL line and the video signal bus." (column 12, lines 33-39). The CL lines 218 and 219 may be

equipped in parallel while maintaining an average distance from the video signal bus to equate the capacitance between said lines and the video signal bus by methods known in the art. For example, clock lines may be equipped vertically coplanar and horizontally parallel to maintain equal distance from the video signal bus. Therefore, Examiner respectfully disagrees and maintains the rejection.

37. The second argument, second full paragraph of Applicant's amendment page 11, states Misawa '936 provides "no assurance that the stray capacitance will actually be cancelled" and "no way to make the load capacitances balanced" is not persuasive. Applicant's arguments in this paragraph are tenuous and wholly unsubstantiated. Therefore, Examiner respectfully disagrees and maintains the rejection.

38. The third argument, third full paragraph of Applicant's amendment page 11, Applicant argues the load means "is a structural element which can take many forms such as the load terminals recited in claim 2 or the capacitor recited in claim 3." However, the limitations of claim 2 or claim 3 are not described in claim 1. Therefore, Examiner respectfully disagrees and maintains the rejection.

39. The fourth argument, fourth full paragraph of Applicant page 11, Applicant argues insufficient motivation to combine Go '566 with Misawa '936. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In*

re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, beyond both references being within the same field of endeavor, Misawa '936 sharply reduces clock noise (column 12 lines 40-45) which would be a concern to one of ordinary skill in the art when using multiple clock lines as in the design of Go '566. A person having ordinary skill in the art at the time of invention would be motivated to combine Go '566 with Misawa '936 for the benefit of reducing such noise. Examiner, therefore, respectfully disagrees with the argument and maintains the rejection.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarvesh J. Nadkarni whose telephone number is 571-270-1541. The examiner can normally be reached on 8:00-5:00 M-Th EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sarvesh J. Nadkarni
Examiner – Art Unit 2629

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER